

Mini-ITX

EMB-945T

EMB-945T

Intel® Core Duo/Solo Processor,

Up to 2.0 GHz

Mini-ITX

Marvell 88E8053 Ethernet

AC 97 Audio & Mini PCI

EMB-945T Manual 2nd Ed.
Mar. 2006

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Packing List

Before you begin installing your card, please make sure that the following materials have been shipped:

- 1 1701440050 44-pin ATA33 Cable
- 1 1700200200 DVI Cable
- 2 1709100201 USB Cable
- 4 1701100206 Serial Port Cable
- 1 1700080180 TV-out Cable
- 2 1709070500 Serial ATA Cable
- 2 1702150150 Serial ATA Power Cable
- 1 9657666600 Jumper Cap
- 1 M166666006 CPU Cooling Fan
- 1 M20852T000 Rear I/O Bracket
- 1 Quick Installation Guide
- 1 Utility CD
- 1 EMB-945T

If any of these items should be missing or damaged, please contact your distributor or sales representative immediately.

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Chapter

1

General Information

1.1 Introduction

The EMB-945T adopts the latest Intel® Core™ Duo processors and Mobile Intel® 945GM Express chipset for better power-management capabilities and enhanced performance. EMB-945T with mobile-optimized Intel dual-core processors is the latest embedded motherboard designed to cope with increasingly heavily work-loaded embedded systems found in POS (Point-of-Sale) machines, automated kiosks, medical instruments, advanced automation for buildings and homes, and gaming machines.

The EMB-945T, based on Intel® Core™ Duo processors, is AAEON's next-generation platform featuring one PCI slot, one PCI-E slot, one Mini PCI slot, six COM ports, six USB 2.0 ports, multiple Digital I/O ports, and Type II CFD storage, providing versatile expansion options for many embedded applications.

The EMB-945T not only keeps the advantages of AAEON's previous embedded motherboard designs, such as the DDRII memory, PCI-Express, and SATA, but also adds more functionality and improved performance. The Front Side Bus is up to 667MHz and graphic performance has been enhanced from 20 to 30%. In addition, the EMB-945T supports DX9L appropriate to the DirectX and LVD/iDCT MPEG2 Hardware Decode.

AAEON is one of the first computer platform vendors to launch an

embedded motherboard with the Intel® Core™ Duo processors in the IPC industry overcoming current limitations of processing speed and power consumption.

1.2 Features

- Supports Socket 478 or Onboard Intel® Core Duo Processors up to 2.0 GHz (T2500)/ Intel® Core Solo Processors
- Two SODIMM Slots Support DDR2 Memory up to 2GB
- Supports 18/24/36/48-bit LVDS Panel, Share Memory up to 224MB with DVMT
- One PCI-E 10/100/1000 Base-TX Ethernet and 6CH AC-97 Audio
- Supports Typell CFD
- One PCI Slot, One PCI-E x 1 Slot and One Mini PCI Socket
- Serial Port x 6, Parallel Port x 1, SATA x 2, ATA33 x 1,USB 2.0 x 6, Digital I/O,
- LCD Inverter Connector with Brightness Control
- Supports Enhanced Intel® SpeedStep Technology
- RoHS Compliance

1.3 Specifications

System

- Processor Supports Socket 478 or onboard Intel® Core Duo Processors up to 2.0 GHz with FSB 667 MHz (T2500)/ Intel® Core Solo Processors
- System Memory DDR II SODIMM Socket x 2, total up to 2GB
- Chipset Intel® 945GM + ICH7M
- I/O Chipset ITE 8712 + Fintek F81216D
- Ethernet Marvell 88E8053 RJ-45 x 1
- BIOS Award Plug & Play BIOS - 512KB ROM
- Watchdog Timer ITE 8712
- H/W Status Monitoring Supports power supply voltages, fan speed and temperature monitoring

- Solid Storage Disk Type II CompactFlash™ slot x 1
- Expansion Interface One PCI slot, One PCI-E(x1), One Mini PCI socket
- Power Requirement ATX (+3.3V, +5V, +12V)
- Board Size 6.7"(L) x 6.7"(W) (170 mm x 170 mm)
- Operating Temperature 32°F~ 140°F (0°C ~ 60°C)

Display

- Chipset Intel® 945GM
- VGA/LCD Controller 1. Intel® 945GM integrated VGA, Share memory up to 224MB with DVMT , LCD supports 18/36-bit LVDS
2. Chrontel 7307 for DVI support
3. Chrontel 7308 for 24/48-bit LVDS support
- TV-out Intel® 945GM integrated

I/O

- MIO Six COM ports:(Four 5x2-pin header, Two D-sub onboard)
COM 1/ 3/ 4/ 5/ 6: RS-232, COM 2:
RS-232/RS-422/RS-485, Provide +5V &
+12V output options on COM2 RI signals.
- IrDA Supports One IrDA header
- Audio Realtek ALC655 CODEC MIC-In/
Line-In/ Line-out, S/PDIF In/Out
- ATA Interface PATA-33 (44Pin) x 1, SATA x 2
- USB Six USB 2.0 Ports
Two 5x2 pin header for Internal,
Two Type-A USB connector for External
- Parallel Port Supports SPP/ EPP/ ECP mode
- K/B and Mouse Mini-DIN PS/2 Keyboard and Mouse
connector x1
- Digital I/O Up to 8 in or 8 out

Chapter

2

Quick Installation Guide

Notice:

The Quick Installation Guide is derived from Chapter 2 of user manual. For other chapters and further installation instructions, please refer to the user manual CD-ROM that came with the product.

OZONE SAFE



RECYCLABLE

2.1 Safety Precautions

Warning!



Always completely disconnect the power cord from your board whenever you are working on it. Do not make connections while the power is on, because a sudden rush of power can damage sensitive electronic components.

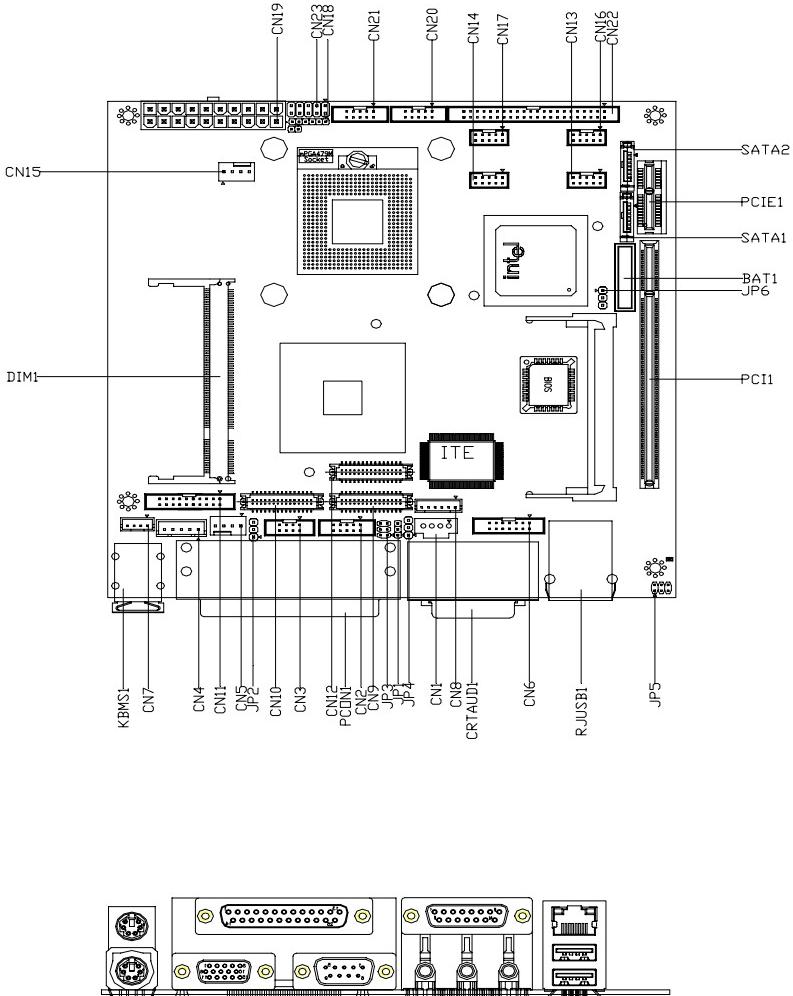
Caution!



Always ground yourself to remove any static charge before touching the board. Modern electronic devices are very sensitive to static electric charges. Use a grounding wrist strap at all times. Place all electronic components on a static-dissipative surface or in a static-shielded bag when they are not in the chassis

2.2 Location of Connectors and Jumpers

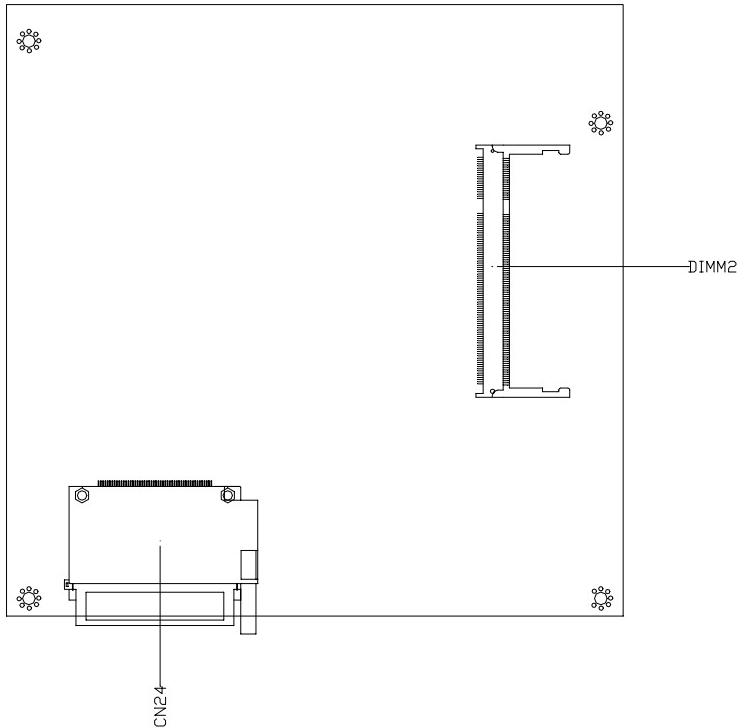
Locating Connectors and Jumpers (Component Side)



Mini ITX

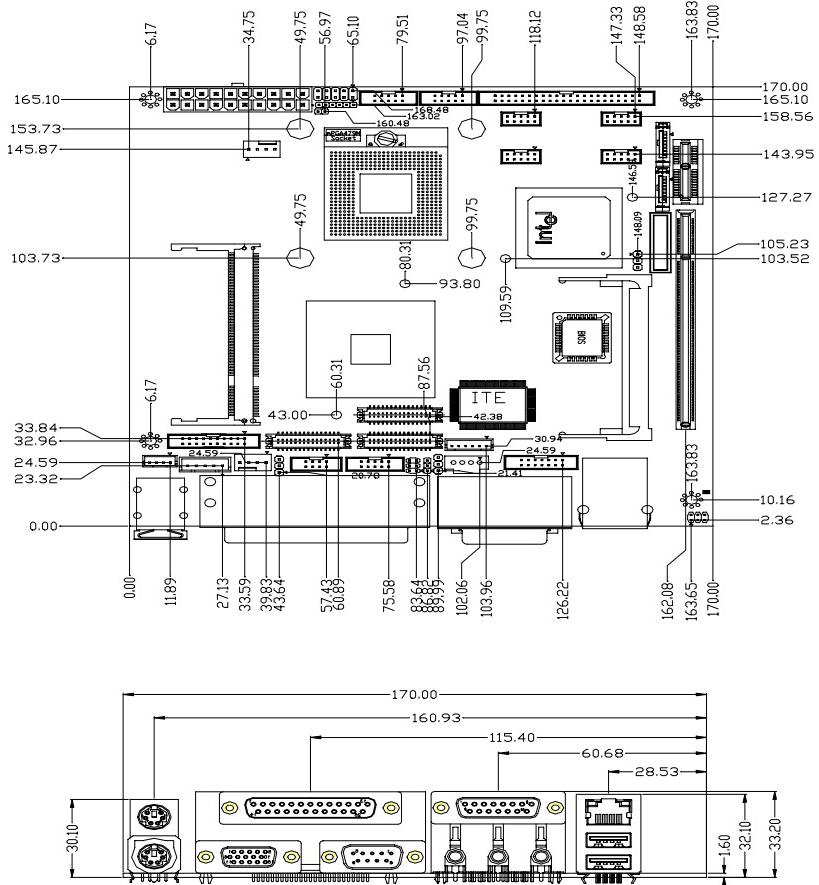
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Locating Connectors and Jumpers (Solder Side)



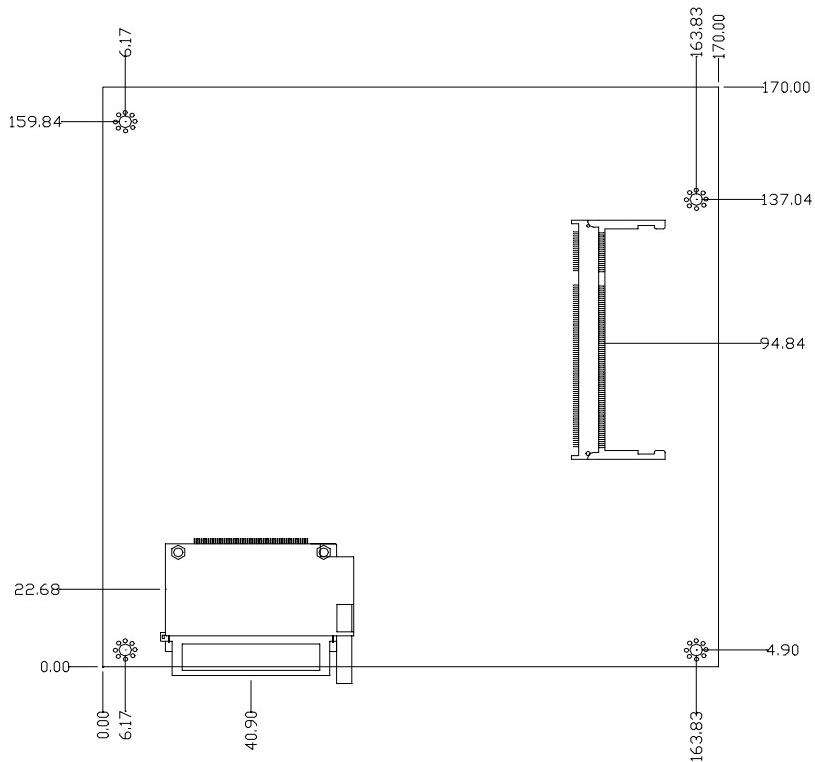
2.3 Mechanical Drawing

Component Side



NOTE:

The height of cooling system depends on customer cooling device.

Solder Side

2.4 List of Jumpers

The board has a number of jumpers that allow you to configure your system to suit your application.

The table below shows the function of each of the board's jumpers:

Jumpers

Label	Function
JP1	LVDS(1)-LCD(CN12) Voltage Selection
JP2	LVDS(2)-LCD(CN10) Voltage Selection
JP3	COM2 Ring/+5V/+12V Selection
JP4	LCD INVERTER Voltage Selection
JP5	Audio Out Selection
JP6	Clear CMOS

2.5 List of Connectors

The board has a number of connectors that allow you to configure your system to suit your application.

The table below shows the function of each of the board's connectors:

Connectors

Label	Function
CN1	CD-IN Connector
CN2	Digital I/O Connector
CN3	TV-Out Connector
CN4	Internal Keyboard Connector
CN5	Fan2 Connector
CN6	Audio 5.1 Channel / SPDIF Connector
CN7	Internal Mouse Connector
CN8	LCD Inverter Connector
CN9	PCI Express Slot For AAEON
CN10	LVDS(2)-LCD Connector for 24/48 bit
CN11	DVI Connector
CN12	LVDS(1)-LCD Connector for 18/36 bit
CN13	COM6 RS-232 Serial Port Connector
CN14	COM3 RS-232 Serial Port Connector
CN15	Fan1 Connector
CN16	COM5 RS-232 Serial Port Connector
CN17	COM4 RS-232 Serial Port Connector
CN18	IrDA Connector
CN19	ATX Power Connector
CN20	USB Connector
CN21	USB Connector
CN22	EIDE Connector
CN23	Front Panel Connector

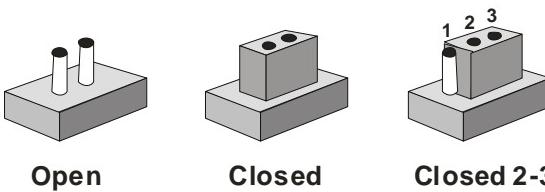
CN24	CompactFlash Slot
CRTAUD1	VGA Display Connector / Audio Connector
KBMS1	PS2 Keyboard / Mouse Connector
PCON1	COM1 RS-232 & COM2 RS-232/422/485 Serial Port
RJUSB1	USB Connector / 10 /100 /1000 Base-Tx Ethernet
MPCI1	Mini PCI Slot
PCI1	PCI Slot
PCIE1	PCI Express Slot
SATA1	Primary Serial ATA Connector
SATA2	Secondary Serial ATA Connector
DIMM1	DDR2 SODIMM Slot
DIMM2	DDR2 SODIMM Slot
COM2	COM2 RS-232 Serial Port Connector

1. The EMB-945T needs different BIOSs to support different bit number LVDS LCDs. The default BIOS only supports 18/36 bit LVDS LCD. If you need to use 24-bit or 48-bit LVDS LCD, please install the BIOS which supports 24-bit or 48-bit LVDS LCD in the CD-ROM.
2. You can refer to the "AAEON BIOS Item Description.pdf" file in the CD for the meaning of each setting in this chapter.

2.6 Setting Jumpers

You configure your card to match the needs of your application by setting jumpers. A jumper is the simplest kind of electric switch. It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To “close” a jumper you connect the pins with the clip.

To “open” a jumper you remove the clip. Sometimes a jumper will have three pins, labeled 1, 2 and 3. In this case you would connect either pins 1 and 2 or 2 and 3.



A pair of needle-nose pliers may be helpful when working with jumpers.

If you have any doubts about the best hardware configuration for your application, contact your local distributor or sales representative before you make any change.

Generally, you simply need a standard cable to make most connections.

2.7 LVDS(1)-LCD(CN12) Voltage Selection (JP1)

JP1	Function
1-2	+5V
2-3	+3.3V (Default)

2.8 LVDS(2)-LCD(CN10) Voltage Selection (JP2)

JP2	Function
1-2	+5V
2-3	+3.3V (Default)

2.9 COM2 Ring/+5V/+12V Selection (JP3)

JP3	Function
1-2	+12V
3-4	+5V
5-6	Ring (Default)

2.10 LCD INVERTER Voltage Selection (JP4)

JP4 LCD	Function
1-2	+5V (Default)
2-3	+12V

2.11 Audio Out Selection (JP5)

JP5	Function
1-3, 2-4	W/ Amplifier
3-5, 4-6	W/O Amplifier (Default)

2.12 Clear CMOS (JP6)

JP6	Function
1-2	Protected (Default)
2-3	Clear

2.13 CD-IN Connector (CN1)

Pin	Signal
1	CD_IN_L
2	CD_GND
3	CD_GND
4	CD_IN_R

2.14 Digital I/O Connector (CN2)

This connector offers 4-pair of digital I/O functions and address is set in BIOS. The default address is 2A1H. The pin definitions are illustrated below:

Pin	Signal		
1	Digital-IN/ OUT	2	Digital-IN/OUT
3	Digital-IN/ OUT	4	Digital-IN/ OUT
5	Digital-IN/ OUT	6	Digital-IN/ OUT
7	Digital-IN/ OUT	8	Digital-IN/ OUT
9	+5V	10	GND

The pin definitions and registers mapping are illustrated below:

4 in / 4 out

Pin8	Pin7	Pin6	Pin5	Pin4	Pin3	Pin2	Pin1
GPI 27	GPI 26	GPI 25	GPI 24	GPO 23	GPO 22	GPO 21	GPO 20
MSB							LSB

8 in

Pin8	Pin7	Pin6	Pin5	Pin4	Pin3	Pin2	Pin1
GPI 27	GPI 26	GPI 25	GPI 24	GPI 23	GPI 22	GPI 21	GPI 20
MSB							

8 out

Pin8	Pin7	Pin6	Pin5	Pin4	Pin3	Pin2	Pin1
GPO 27	GPO 26	GPO 25	GPO 24	GPO 23	GPO 22	GPO 21	GPO 20
MSB							

2.15 TV_Out Connector (CN3)

Pin	Signal	Pin	Signal
1	Y	2	CVBS
3	GND	4	GND
5	C	6	N.C.
7	GND	8	N.C.

2.16 Internal Keyboard Connector (CN4)

Pin	Signal
1	KB_CLK
2	KB_DATA
3	N.C.
4	GND
5	+5V

2.17 Fan2 Connector (CN5)

Pin	Signal
1	GND
2	+12V
3	Speed Sense
4	Speed Control

2.18 Audio 5.1 Channel / SPDIF Connector (CN6)

Pin	Signal	Pin	Signal
1	Front-OUT-R	2	GND
3	Front-OUT-L	4	GND
5	Surr-OUT-R	6	GND
7	Surr-OUT-L	8	GND
9	LFE-OUT	10	GND
11	CNE-OUT	12	GND
13	SPDIF-OUT	14	SPDIF-IN

2.19 Internal Mouse Connector (CN7)

Pin	Signal
1	MS_CLK
2	MS_DATA
3	GND
4	+5V

2.20 LCD Inverter Connector (CN8)

Pin	Signal

1	+5V/+12V
2	+5V/+12V
3	ENBKL
4	Adjust backlight
5	GND
6	GND

2.21 PCI Express Slot For AAEON (CN9)

Pin	Signal	Pin	Signal
1	GND	2	+3.3V
3	PCIE_RXP1	4	+3.3V
5	PCIE_RXN1	6	PCIE_WAKE#
7	GND	8	PCIE_RESET#
9	PCIE1_CLKP	10	+3.3VSB
11	PCIE1_CLKN	12	+3.3VSB
13	GND	14	PCIE_TXP2
15	PCIE_TXP1	16	PCIE_TXN2
17	PCIE_TXN1	18	GND
19	+12V	20	PCIE2_CLKP
21	+12V	22	PCIE2_CLKN
23	SMBDAT	24	GND
25	SMBCLK	26	PCIE_RXP2
27	+3.3V	28	PCIE_RXN2
29	+3.3V	30	GND

2.22 LVDS(2)-LCD Connector (CN10)

Pin	Signal	Pin	Signal
1	ENBKL	2	N.C
3	PPVCC	4	GND
5	LVDS1_TXCLK-	6	LVDS1_TXCLK+
7	PPVCC	8	GND
9	LVDS1_TX0-	10	LVDS1_TX0+
11	LVDS1_TX1-	12	LVDS1_TX1+
13	LVDS1_TX2-	14	LVDS1_TX2+
15	LVDS1_TX3-	16	LVDS1_TX3+
17	I2C_DATA	18	I2C_CLK
19	LVDS2_TX0-	20	LVDS2_TX0+
21	LVDS2_TX1-	22	LVDS2_TX1+
23	LVDS2_TX2-	24	LVDS2_TX2+
25	LVDS2_TX3-	26	LVDS2_TX3+
27	PPVCC	28	GND
29	LVDS2_TXCLK-	30	LVDS2_TXCLK+

2.23 DVI Connector (CN11)

Pin	Signal	Pin	Signal
1	DVI_TX1+	2	LVDS_TX1-
3	GND	4	GND
5	DVI_TXCLK+	6	DVI_TXCLK-
7	GND	8	+5V

9	HotPlug_Detect	10	+5V
11	DVI_TX2+	12	DVI_TX2-
13	GND	14	GND
15	DVI_TX0+	16	DVI_TX0-
17	N.C.	18	N.C.
19	I2C_DATA	20	I2C_CLK

2.24 LVDS(1)-LCD Connector (CN12)

Pin	Signal	Pin	Signal
1	ENBKL	2	N.C
3	PPVCC	4	GND
5	LVDS1_TXCLK-	6	LVDS1_TXCLK+
7	PPVCC	8	GND
9	LVDS1_TX0-	10	LVDS1_TX0+
11	LVDS1_TX1-	12	LVDS1_TX1+
13	LVDS1_TX2-	14	LVDS1_TX2+
15	NC	16	NC
17	I2C_DATA	18	I2C_CLK
19	LVDS2_TX0-	20	LVDS2_TX0+
21	LVDS2_TX1-	22	LVDS2_TX1+
23	LVDS2_TX2-	24	LVDS2_TX2+
25	NC	26	NC
27	PPVCC	28	GND
29	LVDS2_TXCLK-	30	LVDS2_TXCLK+

2.25 COM6 RS-232 Serial Port Connector (CN13)

Pin	Signal	Pin	Signal
1	DCD	2	RXD
3	TXD	4	DTR
5	GND	6	DSR
7	RTS	8	CTS
9	RI	10	N.C.

2.26 COM3 RS-232 Serial Port Connector (CN14)

Pin	Signal	Pin	Signal
1	DCD	2	RXD
3	TXD	4	DTR
5	GND	6	DSR
7	RTS	8	CTS
9	RI	10	N.C.

2.27 Fan1 Connector(CN15)

Pin	Signal
1	GND
2	+12V
3	Speed Sense
4	Speed Control

2.28 COM5 RS-232 Serial Port Connector (CN16)

Pin	Signal	Pin	Signal
1	DCD	2	RXD
3	TXD	4	DTR
5	GND	6	DSR
7	RTS	8	CTS
9	RI	10	N.C.

2.29 COM4 RS-232 Serial Port Connector (CN17)

Pin	Signal	Pin	Signal
1	DCD	2	RXD
3	TXD	4	DTR
5	GND	6	DSR
7	RTS	8	CTS
9	RI	10	N.C.

2.30 IrDA Connector (CN18)

Pin	Signal
1	+5V
2	N.C.
3	IRRX
4	GND
5	IRTX
6	N.C.

2.31 ATX Power Connector (CN19)

Pin	Signal	Pin	Signal
1	+3.3V	11	+3.3V
2	+3.3V	12	-12V
3	GND	13	GND
4	+5V	14	PS_ON
5	GND	15	GND
6	+5V	16	GND
7	GND	17	GND
8	POWER OK	18	-5V
9	+5VSB	19	+5V
10	+12V	20	+5V

2.32 USB Connector (CN20)

Pin	Signal	Pin	Signal
1	+5V	2	GND
3	USBD1-	4	GND
5	USBD1+	6	USBD2+
7	GND	8	USBD2-
9	GND	10	+5V

2.33 USB Connector(CN21)

Pin	Signal	Pin	Signal
1	+5V	2	GND
3	USBD1-	4	GND
5	USBD1+	6	USBD2+

7	GND	8	USBD2-
9	GND	10	+5V

2.34 EIDE Connector (CN22)

CN21 Secondary IDE can't be used after CFD 1 connector has been used. The best way is to use one of them.

Pin	Signal	Pin	Signal
1	IDE RESET	2	GND
3	DATA7	4	DATA8
5	DATA6	6	DATA9
7	DATA5	8	DATA10
9	DATA4	10	DATA11
11	DATA3	12	DATA12
13	DATA2	14	DATA13
15	DATA1	16	DATA14
17	DATA0	18	DATA15
19	GND	20	N.C.
21	REQ	22	GND
23	IO WRITE	24	GND
25	IO READ	26	GND
27	IO READY	28	GND
29	DACK	30	GND
31	IRQ14	32	N.C.
33	ADDR1	34	UDMA DETECT
35	ADDR0	36	ADDR2
37	CS#1	38	CS#3
39	LED	40	GND
41	+5V	42	+5V
43	GND	44	N.C.

2.35 Front Panel Connector (CN23)

Pin	Signal	Pin	Signal
1	Power On Button (-)	2	Power On Button (+)
3	IDE LED (-)	4	IDE LED (+)
5	External Buzzer (-)	6	External Buzzer (+)
7	Power LED (-)	8	Power LED (+)
9	Reset Switch (-)	10	Reset Switch (+)

2.36 COM2 RS-232 Serial Port Connector

Pin	Signal	Pin	Signal
1	DCD (422TXD-/485DATA-)	2	RXD (422RXD+)
3	TXD (422TXD+/485DATA+)	4	DTR (422RXD-)
5	GND	6	DSR
7	RTS	8	CTS
9	RI		

Chapter

3

**Award
BIOS Setup**

3.1 System Test and Initialization

These routines test and initialize board hardware. If the routines encounter an error during the tests, you will either hear a few short beeps or see an error message on the screen. There are two kinds of errors: fatal and non-fatal. The system can usually continue the boot up sequence with non-fatal errors. Non-fatal error messages usually appear on the screen along with the following instructions:

Press <F1> to RESUME

Write down the message and press the F1 key to continue the boot up sequence.

System configuration verification

These routines check the current system configuration against the values stored in the CMOS memory. If they do not match, the program outputs an error message. You will then need to run the BIOS setup program to set the configuration information in memory.

There are three situations in which you will need to change the CMOS settings:

1. You are starting your system for the first time
2. You have changed the hardware attached to your system
3. The CMOS memory has lost power and the configuration information has been erased.

The EMB-945T CMOS memory has an integral lithium battery backup for data retention. However, you will need to replace the complete unit when it finally runs down.

3.2 Award BIOS Setup

Awards BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This type of information is stored in battery-backed CMOS RAM so that it retains the Setup information when the power is turned off.

Entering Setup

Power on the computer and press immediately. This will allow you to enter Setup.



Standard CMOS Features

Use this menu for basic system configuration. (Date, time, IDE, etc.)

Advanced BIOS Features

Use this menu to set the advanced features available on your system.

Advanced Chipset Features

Use this menu to change the values in the chipset registers and optimize your system performance.

Integrated Peripherals

Use this menu to specify your settings for integrated peripherals. (Primary slave, secondary slave, keyboard, mouse etc.)

Power Management Setup

Use this menu to specify your settings for power management. (HDD power down, power on by ring, KB wake up, etc.)

PnP/PCI Configurations

This entry appears if your system supports PnP/PCI.

PC Health Status

This menu allows you to set the shutdown temperature for your system.

Frequency/Voltage Control

Use this menu to specify your settings for auto detect DIMM/PCI clock and spread spectrum.

Load Fail-Safe Defaults

Use this menu to load the BIOS default values for the minimal/stable performance for your system to operate.

Load Optimized Defaults

Use this menu to load the BIOS default values that are factory settings for optimal performance system operations. While AWARD has designated the custom BIOS to maximize performance, the factory has the right to change these defaults to meet their needs.

Set Supervisor/User Password

Use this menu to set Supervisor/User Passwords.

Save and Exit Setup

Save CMOS value changes to CMOS and exit setup.

Exit Without Saving

Abandon all CMOS value changes and exit setup.

1. **The EMB-945T needs different BIOS to support different bit number LVDS LCDs. The default BIOS only supports 18/36 bit LVDS LCD. If you need to use 24-bit or 48-bit LVDS LCD, please install the BIOS which supports 24-bit or 48-bit LVDS LCD in the CD-ROM.**

2. **You can refer to the “AAEON BIOS Item Description.pdf” file in the CD for the meaning of each setting in this chapter.**

Chapter

4

Driver Installation

The EMB-945T comes with a AutoRun CD-ROM that contains all drivers and utilities that can help you to install the driver automatically.

Insert the driver CD, the driver CD-title will auto start and show the installation guide. If not, please follow the sequence below to install the drivers.

Follow the sequence below to install the drivers:

Step 1 – Install Intel Chipset Software Driver

Step 2 – Install VGA Driver

Step 3 – Install LAN Driver

Step 4 – Install Audio Driver

USB 2.0 Drivers are available for download using Windows® Update for both Windows® XP and Windows® 2000. For additional information regarding USB 2.0 support in Windows® XP and Windows® 2000, please visit www.microsoft.com/hwdev/usb/.

Please read instructions below for further detailed installations.

4.1 Installation:

Insert the EMB-945T CD-ROM into the CD-ROM drive. And install the drivers from Step 1 to Step 4 in order.

Step 1 – Install Intel INF Update for Windows 2000/XP

1. Click on the **Chip** folder and then double click on the **infinst_autol.exe**.
2. Follow the instructions that the window shows
3. The system will help you install the driver automatically
4. Please re-start your computer

Step 2 – Install VGA Driver

1. Click on the **VGA** folder and then double click on the **setup.exe**.
2. Follow the instructions that the window shows
3. The system will help you install the driver automatically
4. Please re-start your computer

Step 3 – Install LAN Driver

1. Click on the **LAN Driver** folder
2. Click on the Windows folder and then double click on **SetupYukonWin.exe**
3. Follow the instructions that the window shows
4. The system will help you install the driver automatically

Step 4 – Install Realtek AC97 codec Driver

1. Click on the **AC97** folder
2. Click on **Win98ME2KXP** folder and then double click on **wdm_a371.exe**
3. Follow the instructions that the window shows
4. The system will help you install the driver automatically

Note:

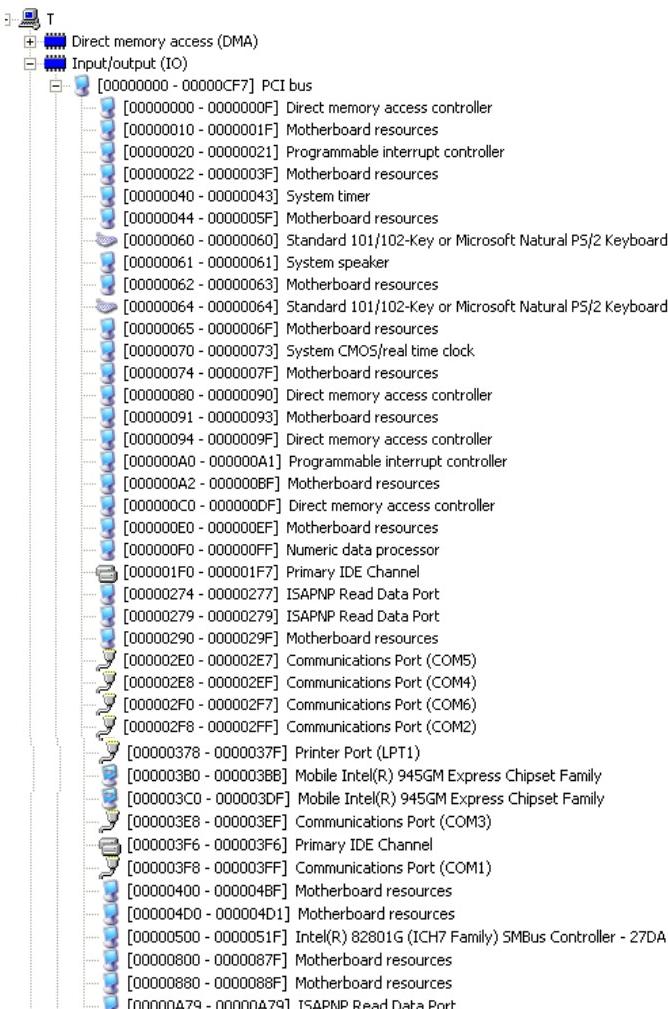
Under the Window OS environment, if the CRT connector is connected to display monitor by the data switch device, the user need to set the color and resolution from Intel Graphic utility (VGA driver) instead of setting from the control panel in case of the wrong display appearance.

Appendix

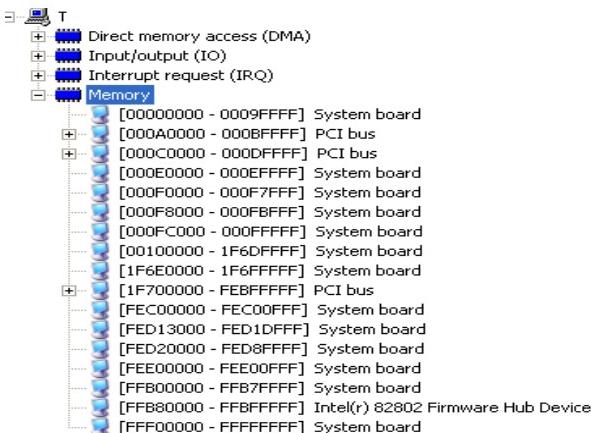
A

I/O Information

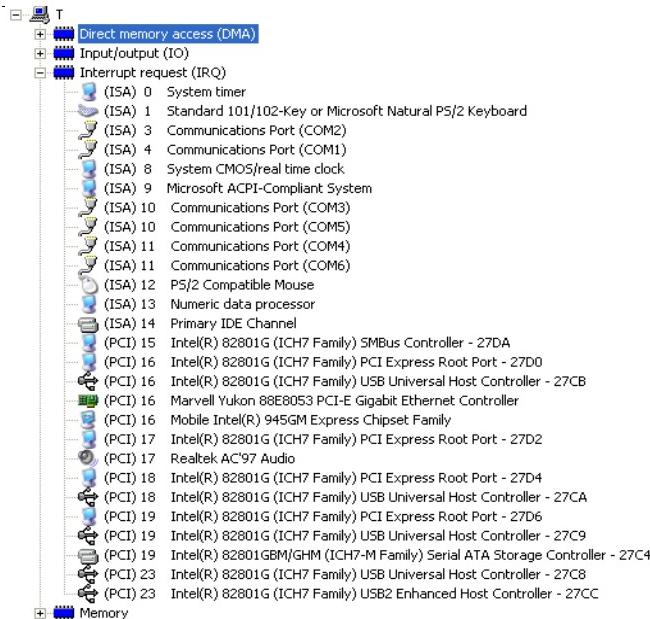
A.1 I/O Address Map



A.2 Memory Address Map



A.3 IRQ Mapping Chart



A.4 DMA Channel Assignments



Appendix

B

Programming the Watchdog Timer

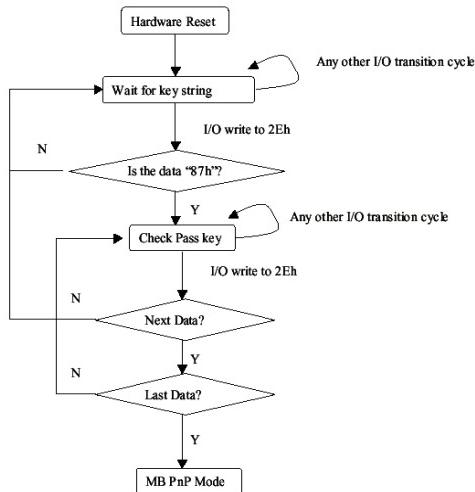
B.1 Programming

EMB-945T utilizes ITE 8712 chipset as its watchdog timer controller.

Below are the procedures to complete its configuration and the AAEON intial watchdog timer program is also attached based on which you can develop customized program to fit your application.

Configuring Sequence Description

After the hardware reset or power-on reset, the ITE 8712 enters the normal mode with all logical devices disabled except KBC. The initial state (enable bit) of this logical device (KBC) is determined by the state of pin 121 (DTR1#) at the falling edge of the system reset during power-on reset.



There are three steps to complete the configuration setup: (1) Enter the MB PnP Mode; (2) Modify the data of configuration registers; (3) Exit the MB PnP Mode. Undesired result may occur if the MB PnP Mode is not exited normally.

(1) Enter the MB PnP Mode

To enter the MB PnP Mode, four special I/O write operations are to be performed during Wait for Key state. To ensure the initial state of the key-check logic, it is necessary to perform four write operations to the Special Address port (2EH). Two different enter keys are provided to select configuration ports (2Eh/2Fh) of the next step.

Address Port	Data Port
87h, 01h, 55h, 55h:	2Eh 2Fh

(2) Modify the Data of the Registers

All configuration registers can be accessed after entering the MB PnP Mode. Before accessing a selected register, the content of Index 07h must be changed to the LDN to which the register belongs, except some Global registers.

(3) Exit the MB PnP Mode

Set bit 1 of the configure control register (Index=02h) to 1 to exit the MB PnP Mode.

WatchDog Timer Configuration Registers

LDN Index R/W	Reset Configuration Register or Action
All 02H W N/A	Configure Control
07H 71H R/W 00H	WatchDog Timer Control Register
07H 72H R/W 00H	WatchDog Timer Configuration Register
07H 73H R/W 00H	WatchDog Timer Time-out Value Register

Configure Control (Index=02h)

This register is write only. Its values are not sticky; that is to say, a hardware reset will automatically clear the bits, and does not require the software to clear them.

Bit	Description
7-2	Reserved
1	Returns to the Wait for Key state. This bit is used when the configuration sequence is completed
0	Resets all logical devices and restores configuration registers to their power-on states.

WatchDog Timer Control Register (Index=71h, Default=00h)

Bit	Description
7	WDT is reset upon a CIR interrupt
6	WDT is reset upon a KBC (mouse) interrupt
5	WDT is reset upon a KBC (keyboard) interrupt
4	WDT is reset upon a read or a write to the Game Port base address
3-2	Reserved
1	Force Time-out. This bit is self-clearing
0	WDT Status
	1: WDT value reaches 0.
	0: WDT value is not 0

WatchDog Timer Configuration Register (Index=72h,**Default=00h)****Bit Description**

7 WDT Time-out value select

1: Second

0: Minute

6 WDT output through KRST (pulse) enable

5-4 Reserved

3-0 Select the interrupt level^{Note} for WDT**WatchDog Timer Time-out Value Register (Index=73h,****Default=00h)****Bit Description**

7-0 WDT Time-out value 7-0

B.2 IT8712 Watchdog Timer Initial Program

```
.MODEL SMALL
```

```
.CODE
```

Main:

```
CALL Enter_Configuration_mode
```

```
CALL Check_Chip
```

```
mov cl, 7
```

```
call Set_Logic_Device
```

```
;time setting
```

```
mov cl, 10 ; 10 Sec
```

```
dec al
```

Watch_Dog_Setting:

```
;Timer setting
```

```
mov al, cl
```

```
mov cl, 73h
```

```
call Superio_Set_Reg
```

```
;Clear by keyboard or mouse interrupt
```

```
mov al, 0f0h
```

```
mov cl, 71h
```

```
call Superio_Set_Reg
```

```
;unit is second.
```

```
mov al, 0C0H
```

```
mov cl, 72h
```

```
call Superio_Set_Reg
```

```
; game port enable  
mov cl, 9  
call Set_Logic_Device
```

```
Initial_OK:  
CALL Exit_Configuration_Mode  
MOV AH,4Ch  
INT 21h
```

```
Enter_Configuration_Mode PROC NEAR  
MOV SI,WORD PTR CS:[Offset Cfg_Port]
```

```
MOV DX,02Eh  
MOV CX,04h  
Init_1:  
MOV AL,BYTE PTR CS:[SI]  
OUT DX,AL  
INC SI  
LOOP Init_1  
RET
```

```
Enter_Configuration_Mode ENDP
```

```
Exit_Configuration_Mode PROC NEAR  
MOV AX,0202h  
CALL Write_Configuration_Data
```

RET

Exit_Configuration_Mode ENDP

Check_Chip PROC NEAR

MOV AL,20h

CALL Read_Configuration_Data

CMP AL,87h

JNE Not_Initial

MOV AL,21h

CALL Read_Configuration_Data

CMP AL,12h

JNE Not_Initial

Need_Initial:

STC

RET

Not_Initial:

CLC

RET

Check_Chip ENDP

Read_Configuration_Data PROC NEAR

MOV DX,WORD PTR CS:[Cfg_Port+04h]

OUT DX,AL

```
MOV DX,WORD PTR CS:[Cfg_Port+06h]
```

```
IN AL,DX
```

```
RET
```

```
Read_Configuration_Data ENDP
```

```
Write_Configuration_Data PROC NEAR
```

```
MOV DX,WORD PTR CS:[Cfg_Port+04h]
```

```
OUT DX,AL
```

```
XCHG AL,AH
```

```
MOV DX,WORD PTR CS:[Cfg_Port+06h]
```

```
OUT DX,AL
```

```
RET
```

```
Write_Configuration_Data ENDP
```

```
Superio_Set_Reg proc near
```

```
push ax
```

```
MOV DX,WORD PTR CS:[Cfg_Port+04h]
```

```
mov al,cl
```

```
out dx,al
```

```
pop ax
```

```
inc dx
```

```
out dx,al
```

```
ret
```

```
Superio_Set_Reg endp.
```

```
Set_Logic_Device proc near
```

```
push ax  
push cx  
xchg al,cl  
mov cl,07h  
call Superio_Set_Reg  
pop cx  
pop ax  
ret  
Set_Logic_Device endp
```

;Select 02Eh->Index Port, 02Fh->Data Port
Cfg_Port DB 087h,001h,055h,055h

DW 02Eh,02Fh

END Main

Note: Interrupt level mapping

0Fh-Dh: not valid

0Ch: IRQ12

03h: IRQ3

02h: not valid

01h: IRQ1

00h: no interrupt selected